Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10	((program$6 adj2 item$2) and parameter$1) and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:26
L2	8	(("PLD" or "PLDs") and (FPGA or "FPGAs") and @ad<"20010727") and ("programmable item" or "programmable items" or "programmable data")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:27
L3	5	generat$4 same (program$6 adj2 (item$2 or data)) same parameter$1 and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:27
L4	10	(generat$3 same (("net list" or "net lists" or netlist$1 or (program$6 adj2 item$2)) and parameter$1) and @ad<"20010727") and ("frequency parameter" or "frequency parameters" or "time parameter" or "time parameters")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:28
L5	121	714/53.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:45
L6	44	error$1 and (programmable adj2 field$1) and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:45
L7	10	(error$1 and (first adj2 field$1) and (second adj2 field$1) and ("programmable logic" adj2 devic$2) and @ad<"20010727") and (third adj2 field$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:29
L8	1	6 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:48
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L11	46	5 and error near detection	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:30
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L13	50696	"714"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:51
L14	1	7 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:51
L15	14	stor$4 and "non-programmable" near10 field$ and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:33
L16	73	("frequency parameter" or "frequency parameters" or "time parameter" or "time parameters") and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:53
L17	143	extract$3 same error$1 adj2 detect$5 and extract$3 same compress$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:53
L18	0	7 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:54
L19	59	("non-programmable" or "not programmable") and ((first or second or third or fourth) near2 field) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:31
L20	1	7 and 19	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:54
L21	22	generat$3 and (huffman adj2 encod$3 or huffman adj2 tree or huffman adj2 hierarchy) and error and @ad<"20000809" and (("programmable logic" adj2 devic$2) or ("PLD" or "PLDs"))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 11:55

L22	73	("frequency parameter" or "frequency parameters" or "time parameter" or "time parameters") and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:17
L23	68	"707"/$.ccls. and parameter$1 and ("programmable logic" adj2 devic$2) and @ad<"20010727"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/09 12:33

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A **field-programmable** gate array or **FPGA** is a semiconductor **device** containing ... ability to re-**program** in the **field** to fix bugs, and lower **non**-recurring ...
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1 Security on FPGAs: State-of-the-art implementations and attacks

Thomas Wollinger, Jorge Guajardo, Christof Paar

August 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 3

Publisher: ACM Press

Full text available: pdf(296.79 KB) Additional Information: full citation, abstract, references, index terms

In the last decade, it has become apparent that embedded systems are integral parts of our every day lives. The wireless nature of many embedded applications as well as their omnipresence has made the need for security and privacy preserving mechanisms particularly important. Thus, as field programmable gate arrays (FPGAs) become integral parts of embedded systems, it is imperative to consider their security as a whole. This contribution provides a state-of-the-art description of security issues ...

Keywords: Cryptography, FPGA, attacks, cryptographic applications, reconfigurable hardware, reverse engineering, security

2 Developing critical systems with PLD components

Adrian Hilton, Jon G. Hall

September 2005 **Proceedings of the 10th international workshop on Formal methods for industrial critical systems FMICS '05**

Publisher: ACM Press

Full text available: pdf(113.16 KB) Additional Information: full citation, abstract, references, index terms

Understanding the roles that rigour and formality can have in the design of critical systems is critical to anyone wishing to contribute to their development. Whereas knowledge of these issues is good in software development, in the use of hardware -- specifically programmable logic devices (PLDs) and the combination of PLDs and software -- the issues are less well known. Indeed, even in industry there are many differences between current and recommended practice and engineering opinion differs ...

Keywords: CSP, FPGA, PLD, parallel, process algebra, programmable hardware, programmable logic, programming languages, survey

3 Logic synthesis and mapping: Verifying the correctness of FPGA logic synthesis algorithms

Boris Ratchev, Mike Hutton, Gregg Baeckler, Babette van Antwerpen
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(146.65 KB) Additional Information: full citation, abstract, references, index terms

Though verification is significantly easier for FPGA-based digital systems than for ASIC or full-custom hardware, there are nonetheless many places for errors to occur.In this paper we discuss the verification problem for FPGAs and describe several methods for verifying end-to-end correctness of synthesis algorithms, a particularly complex portion of the CAD flow. Though the primary contribution of this paper is the analysis of the overall problem, we also give an algorithm for the automatic gen ...

Keywords: FPGA, programmable logic, synthesis, test, verification

4 New directions for programmable devices: Soft error rate estimation and mitigation for SRAM-based FPGAs
Ghazanfar Asadi, Mehdi B. Tahoori
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(241.45 KB) Additional Information: full citation, abstract, references, index terms

FPGA-based designs are more susceptible to single-event upsets (SEUs) compared to ASIC designs. Soft error rate (SER) estimation is a crucial step in the design of soft error tolerant schemes to balance reliability, performance, and cost of the system. Previous techniques on FPGA SER estimation are based on time-consuming fault injection and simulation methods.In this paper, we present an analytical approach to estimate the failure rate of designs mapped into FPGAs. Experimental results show tha ...

Keywords: SRAM-based FPGA, error recovery, soft error rate estimation

5 Interconnect prediction for programmable logic devices
Michael Hutton
March 2001 **Proceedings of the 2001 international workshop on System-level interconnect prediction**
Publisher: ACM Press
Full text available: pdf(288.08 KB) Additional Information: full citation, abstract, references, citings, index terms

Classical interconnect prediction would seem to be a perfect fit for the design of programmable logic architectures (PLDs). Yet theoretical models such as those based on Rent's Rule are usually only used for rough estimates in the early stages of an architecture development. In practice, empirical methods (evaluation via many test designs) dominate the evaluation of fitting and performance for PLD architectures.The primary reasons for this gap between theory and practice are th ...

Keywords: architecture, interconnect prodiction, programmable logic device, wireability

6 Error detection for adaptive computing architectures in spacecraft applications
David Brodrick, Anwar Dawood, Neil Bergmann, Melanie Wark
January 2001 **Australian Computer Science Communications , Proceedings of the 6th Australasian conference on Computer systems architecture ACSAC '01**, Volume 23 Issue 4
Publisher: IEEE Computer Society , IEEE Computer Society Press

Full text available: pdf(803.02 KB) Additional Information: full citation, abstract, references
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The Australian FedSat satellite will incorporate a payload to validate the use of adaptive computing architectures in spacecraft applications. The technology has many exciting benefits for deployment in spacecraft, but the space environment also represents unique challenges which must be addressed. An important consideration is that modern SRAM Field Programmable Gate Arrays (FPGAs), such as the Xilinx 4000 device used on FedSat, are vulnerable to a range of radiation induced errors. A system is ...

7 A memory coherence technique for online transient error recovery of FPGA configurations

Wei-Je Huang, Edward J. McCluskey
February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(271.54 KB) Additional Information: full citation, abstract, references, index terms

The partial reconfiguration feature of some of the current-generation Field Programmable Gate Arrays (FPGAs) can improve dependability by detecting and correcting errors in on-chip configuration data. Such an error recovery process can be executed online with minimal interference of user applications. However, because Look-up Tables (LUTs) in Configurable Logic Blocks (CLBs) of FPGAs can also implement memory modules for user applications, a memory coherence issue arises such that memory ...

Keywords: FPGA, error recovery, fault tolerance, memory coherence

8 Special session on reconfigurable computing: Designing and testing fault-tolerant techniques for SRAM-based FPGAs

Fernanda Lima Kastensmidt, Gustavo Neuberger, Luigi Carro, Ricardo Reis
April 2004 **Proceedings of the 1st conference on Computing frontiers**
Publisher: ACM Press
Full text available: pdf(390.51 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses fault-tolerant techniques for SRAM-based FPGAs. These techniques can be based on circuit level modifications, with obvious modifications in the programmable architecture, or they can be implemented at the high-level description, without modification in the FPGA architecture. The high-level method presented in this work is based on Triple Modular Redundancy (TMR) and a combination of Duplication Modular Redundancy (DMR) with Concurrent Error Detection (CED) techniques, which ...

Keywords: FPGA, fault-tolerance

9 Techniques for reconfigurable logic applications: Designing fault tolerant systems into SRAM-based FPGAs

Fernanda Lima, Luigi Carro, Ricardo Reis
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(238.49 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses high level techniques for designing fault tolerant systems in SRAM-based FPGAs, without modification in the FPGA architecture. Triple Modular Redundancy (TMR) has been successfully applied in FPGAs to mitigate transient faults, which are likely to occur in space applications. However, TMR comes with high area and power dissipation

penalties. The new technique proposed in this paper was specifically developed for FPGAs to cope with transient faults in the user combinational a ...

Keywords: FPGA, fault-tolerance

10 Efficient error detection, localization, and correction for FPGA-based debugging

John Lach, William H. Mangione-Smith, Miodrag Potkonjak
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(86.05 KB) Additional Information: full citation, abstract, references, index terms

Simulations for modern designs are often performed on Field Programmable Gate Array technology in a functional test and debugging process known as emulation, allowing for more complex simulations than possible in software. One drawback to emulation is the lengthy time spent in the back-end CAD tools for each debugging iteration, including debugging changes and the introduction of control and observation logic. We have developed a technique that confines the re-place-and-route area to only t ...

11 Prototyping, verification, and test: Reducing pin and area overhead in fault-tolerant FPGA-based designs

Fernanda Lima, Luigi Carro, Ricardo Reis
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(328.13 KB) Additional Information: full citation, abstract, references, index terms

This paper proposes a new high-level technique for designing fault tolerant systems in SRAM-based FPGAs, without modifications in the FPGA architecture. Traditionally, TMR has been successfully applied in FPGAs to mitigate transient faults, which are likely to occur in space applications. However, TMR comes with high area and power dissipation penalties. The proposed technique was specifically developed for FPGAs to cope with transient faults in the user combinational and sequential logic, while ...

Keywords: FPGA, fault-tolerance

12 ASIC design in nanometer era - dead or alive?: Exploring regular fabrics to optimize the performance-cost trade-off

L. Pileggi, H. Schmit, A. J. Strojwas, P. Gopalakrishnan, V. Kheterpal, A. Koorapaty, C. Patel, V. Rovner, K. Y. Tong
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(319.99 KB) Additional Information: full citation, abstract, references, citings, index terms

While advances in semiconductor technologies have pushed achievable scale and performance to phenomenal limits for ICs, nanoscale physical realities dictate IC production based on what we can afford. We believe that IC design and manufacturing can be made more affordable, and reliable, by removing some design and implementation flexibility and enforcing new forms of design regularity. This paper discusses some of the trade-offs to consider for determination of how much regularity a particular IC ...

Keywords: cost, integrated circuits, performance, regularity

13 Timing-driven placement for hierarchical programmable logic devices

Michael Hutton, Khosrow Adibsamii, Andrew Leaver

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(213.63 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we discuss new techniques for timing-driven placement and adaptive delay computation for hierarchical PLD architectures.Our algorithm follows the natural recursive k-way partitioning-based approach to placement on such devices. Our contributions include a specification of the overall TDC (timing-driven compilation) algorithm, an analysis of heuristics such as a variant of multi-start partitioning, a new method for adaptive delay computation, and a discussion of the ...

Keywords: CPLD, FPGA, algorithm, heuristic algorithm, partitioning, placement, programmable logic, timing-driven placement

14 Efficiently supporting fault-tolerance in FPGAs

John Lach, William H. Mangione-Smith, Miodrag Potkonjak

March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, citings, index terms

While system reliability is conventionally achieved through component replication, we have developed a fault-tolerance approach for FPGA-based systems that comes at a reduced cost in terms of design time, volume, and weight. We partition the physical design into a set of tiles. In response to a component failure, we capitalize on the unique reconfiguration capabilities of FPGAs and replace the affected tile with a functionally equivalent tile that does not rely on the faulty component. Unli ...

Keywords: FPGA, fault-tolerance

15 Evaluation of FPGA resources for built-in self-test of programmable logic blocks

Charles Stroud, Ping Chen, Srinivasa Konala, Miron Abramovici

February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(49.07 KB) Additional Information: full citation, references, citings, index terms

16 Design methodology for PicoRadio networks

J. da Silva, J. Shamberger, M. Ammer, C. Guo, S. Li, R. Shah, T. Tuan, M. Sheets, J. Rabaey, B. Nikolic, A. Sangiovanni-Vincentelli, P. Wright

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Press

Full text available: pdf(328.60 KB) Additional Information: full citation, references, index terms

17 A design flow for partially reconfigurable hardware

Ian Robertson, James Irvine

May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2
Publisher: ACM Press
Full text available: pdf(698.30 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a top-down designer-driven design flow for creating hardware that exploits partial run-time reconfiguration. Computer-aided design (CAD) tools are presented, which complement conventional FPGA design environments to enable the specification, simulation (both functional and timing), synthesis, automatic placement and routing, partial configuration generation and control of partially reconfigurable designs. Collectively these tools constitute the dynamic circuit switching CAD f ...

Keywords: FPGA, Viterbi decoder, configuration control, dynamically reconfigurable logic (DRL), power estimation, run-time reconfiguration (RTR)

18 Balancing performance and flexibility with hardware support for network architectures
Ilija Hadžić, Jonathan M. Smith
November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4
Publisher: ACM Press
Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

19 Content inspection: High-throughput linked-pattern matching for intrusion detection systems
Zachary K. Baker, Viktor K. Prasanna
October 2005 **Proceedings of the 2005 symposium on Architecture for networking and communications systems ANCS '05**
Publisher: ACM Press
Full text available: pdf(300.66 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a hardware architecture for highly efficient intrusion detection systems. In addition, a software tool for automatically generating the hardware is presented.Intrusion detection for network security is a compute-intensive application demanding high system performance. By moving both the string matching and the linking of multi-part rules to hardware, our architecture leaves the host system free for higher-level analysis. The tool automates the creation of efficient Field Prog ...

Keywords: network intrusion detection, string matching

20 Poster session: An FPGA architecture with built-in error correction capability
P. K. Lala, B. Kiran Kumar
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The use of very deep submicron technology makes VLSI-based digital systems more susceptible to transient or soft errors, and thus compromises their reliability. This paper proposes an FPGA architecture inspired by the human immune system that allows tolerance of transient errors. The architecture is composed of a two-dimensional array of identical functional cells with different genetic codes. These codes are chosen based on the required functions to be performed by the functional cells. An erro ...

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1 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**

Publisher: IBM Press

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

2 Query evaluation techniques for large databases

Goetz Graefe

June 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 2

Publisher: ACM Press

Full text available: pdf(9.37 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Database management systems will continue to manage large data volumes. Thus, efficient algorithms for accessing and manipulating large sets and sequences will be required to provide acceptable performance. The advent of object-oriented and extensible database systems will not solve this problem. On the contrary, modern data models exacerbate the problem: In order to manipulate large sets of complex objects as efficiently as today's database systems manipulate simple records, query-processi ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, extensible database systems, iterators, object-oriented database systems, operator model of parallelization, parallel algorithms, relational database systems, set-matching algorithms, sort-hash duality

3 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Publisher: ACM Press

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

4 Pitfalls and safeguards in real-time digital systems with emphasis on programming
W. A. Hosier
March 1987 **Proceedings of the 9th international conference on Software Engineering**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.98 MB) Additional Information: full citation, abstract, references, citings, index terms

Real-time digital systems are largely a technical innovation of the past decade, but they appear destined to become more wide spread in the future. They monitor or control a real physical environment, such as an air-traffic situation, as distinguished from simulating that environment on an arbitrary time scale. The complexity and rapid variation of such an environment necessitates use of a fast and versatile central-control device, a role well suited to digital computers. The usual system w ...

5 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science
William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young
March 1968 **Communications of the ACM**, Volume 11 Issue 3
Publisher: ACM Press
Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

6 Graphics Programming Using the Core System
R. Daniel Bergeron, Peter R. Bono, James D. Foley
December 1978 **ACM Computing Surveys (CSUR)**, Volume 10 Issue 4
Publisher: ACM Press
Full text available: pdf(2.92 MB) Additional Information: full citation, references, citings, index terms

7 Proceedings of the SIGNUM conference on the programming environment for development of numerical software
March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1
Publisher: ACM Press
Full text available: pdf(5.02 MB) Additional Information: full citation

8 Data base directions: the next steps
John L. Berg
November 1976 **ACM SIGMOD Record , ACM SIGMIS Database**, Volume 8 , 8 Issue 4 , 2
Publisher: ACM Press
Full text available: Additional Information:

pdf(9.95 MB) full citation, abstract

What information about data base technology does a manager need to make prudent decisions about using this new technology? To provide this information the National Bureau of Standards and the Association for Computing Machinery established a workshop of approximately 80 experts in five major subject areas. The five subject areas were auditing, evolving technology, government regulations, standards, and user experience. Each area prepared a report contained in these proceedings. The proceedings p ...

Keywords: DBMS, auditing, cost/benefit analysis, data base, data base management, government regulation, management objectives, privacy, security, standards, technology assessment, user experience

9 Work-in-progress session on innovative topics: First results with eBlocks: embedded systems building blocks

Susan Cotterell, Frank Vahid, Walid Najjar, Harry Hsieh

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Publisher: ACM Press

Full text available: pdf(433.19 KB) Additional Information: full citation, abstract, references, index terms

We describe our first efforts to develop a set of off-the-shelf hardware components that ordinary people could connect to build a simple but useful class of embedded systems. The class of systems, which we call monitor/control systems, is composed primarily of sensors - light, motion, sound, contact, and other types - and output devices - light-emitting diodes, beeping speakers, or even electric relays that control electric appliances like lamps. For example, one monitor/control system would det ...

Keywords: embedded systems, intelligent homes, networks

10 IS '97: model curriculum and guidelines for undergraduate degree programs in information systems

Gordon B. Davis, John T. Gorgone, J. Daniel Couger, David L. Feinstein, Herbert E. Longenecker

December 1996 **ACM SIGMIS Database , Guidelines for undergraduate degree programs on Model curriculum and guidelines for undergraduate degree programs in information systems IS '97**, Volume 28 Issue 1

Publisher: ACM Press

Full text available: pdf(7.24 MB) Additional Information: full citation, citings

11 The FINITE STRING Newsletter: Abstracts of current literature

Computational Linguistics Staff

January 1987 **Computational Linguistics**, Volume 13 Issue 1-2

Publisher: MIT Press

Full text available: pdf(6.15 MB) Additional Information: full citation

Publisher Site

12 Conference abstracts

January 1977 **Proceedings of the 5th annual ACM computer science conference**

Publisher: ACM Press

Full text available: pdf(3.14 MB) Additional Information: full citation, abstract, index terms

One problem in computer program testing arises when errors are found and corrected after a portion of the tests have run properly. How can it be shown that a fix to one area of the code does not adversely affect the execution of another area? What is needed is a quantitative method for assuring that new program modifications do not introduce new errors into the code. This model considers the retest philosophy that every program instruction that could possibly be reached and tested from the ...

13 Evolution of Data-Base Management Systems

James P. Fry, Edgar H. Sibley
January 1976 **ACM Computing Surveys (CSUR)**, Volume 8 Issue 1
Publisher: ACM Press
Full text available: pdf(2.63 MB) Additional Information: full citation, references, citings, index terms

14 Revised Report of the Algorithmic Language Algol 68

A. van Wijngaarden
August 1981 **ALGOL Bulletin**, Issue Sup 47
Publisher: Computer History Museum
Full text available: pdf(9.20 MB) Additional Information: full citation, index terms

15 Client-server computing in mobile environments

Jin Jing, Abdelsalam Sumi Helal, Ahmed Elmagarmid
June 1999 **ACM Computing Surveys (CSUR)**, Volume 31 Issue 2
Publisher: ACM Press
Full text available: pdf(233.31 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Recent advances in wireless data networking and portable information appliances have engendered a new paradigm of computing, called mobile computing, in which users carrying portable devices have access to data and information services regardless of their physical location or movement behavior. In the meantime, research addressing information access in mobile environments has proliferated. In this survey, we provide a concrete framework and categorization of the various way ...

Keywords: application adaptation, cache invalidation, caching, client/server, data dissemination, disconnected operation, mobile applications, mobile client/server, mobile compuing, mobile data, mobility awareness, survey, system application

16 System support for pervasive applications

Robert Grimm, Janet Davis, Eric Lemar, Adam Macbeth, Steven Swanson, Thomas Anderson, Brian Bershad, Gaetano Borriello, Steven Gribble, David Wetherall
November 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 4
Publisher: ACM Press
Full text available: pdf(1.82 MB) Additional Information: full citation, abstract, references, index terms

Pervasive computing provides an attractive vision for the future of computing. Computational power will be available everywhere. Mobile and stationary devices will dynamically connect and coordinate to seamlessly help people in accomplishing their tasks. For this vision to become a reality, developers must build applications that constantly adapt to a highly dynamic computing environment. To make the developers' task feasible, we present a system architecture for pervasive computing, called & ...

Keywords: Asynchronous events, checkpointing, discovery, logic/operation pattern, migration, one.world, pervasive computing, structured I/O, tuples, ubiquitous computing

17 Document Formatting Systems: Survey, Concepts, and Issues
Richard Furuta, Jeffrey Scofield, Alan Shaw
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Publisher: ACM Press
Full text available: pdf(5.36 MB) Additional Information: full citation, references, citings, index terms

18 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Publisher: ACM Press
Full text available: pdf(5.28 MB) Additional Information: full citation

19 Frontmatter (TOC, Letters, Philosophy of computer science, Interviewers needed, Taking software requirements creation from folklore to analysis, SW components and product lines: from business to systems and technology, Software engineering survey)
September 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 5
Publisher: ACM Press
Full text available: pdf(1.98 MB) Additional Information: full citation

20 Frontmatter (TOC, Letters, Election results, Software Reliability Resources!, Computing Curricula 2004 and the Software Engineering Volume SE2004, Software Reuse Research, ICSE 2005 Forward)
July 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 4
Publisher: ACM Press
Full text available: pdf(6.19 MB) Additional Information: full citation

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1 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

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Publisher: IBM Press

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

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2 Proceedings of the SIGNUM conference on the programming environment for development of numerical software

March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1

Publisher: ACM Press

Full text available: pdf(5.02 MB) Additional Information: full citation

3 Status report of the graphic standards planning committee

Computer Graphics staff

August 1979 **ACM SIGGRAPH Computer Graphics**, Volume 13 Issue 3

Publisher: ACM Press

Full text available: pdf(15.01 MB) Additional Information: full citation, references, citings

4 Special issue: AI in engineering

D. Sriram, R. Joobbani

April 1985 **ACM SIGART Bulletin**, Issue 92

Publisher: ACM Press

Full text available: pdf(8.79 MB) Additional Information: full citation, abstract

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the SIGART newsletter and notices posted over the ARPAnet. The interest being shown in this area is reflected in the sixty papers received from over six countries. About half the papers were received over the computer network.

5 Special issue on knowledge representation

Ronald J. Brachman, Brian C. Smith
February 1980 **ACM SIGART Bulletin**, Issue 70
Publisher: ACM Press
Full text available: pdf(13.13 MB) Additional Information: full citation, abstract

In the fall of 1978 we decided to produce a special issue of the SIGART Newsletter devoted to a survey of current knowledge representation research. We felt that there were twe useful functions such an issue could serve. First, we hoped to elicit a clear picture of how people working in this subdiscipline understand knowledge representation research, to illuminate the issues on which current research is focused, and to catalogue what approaches and techniques are currently being developed. Secon ...

6 Status report of the graphic standards planning committee of ACM/SIGGRAPH: State-of-the-art of graphic software packages

Compuater Graphics staff
September 1977 **ACM SIGGRAPH Computer Graphics**, Volume 11 Issue 3
Publisher: ACM Press
Full text available: pdf(9.03 MB) Additional Information: full citation, references

7 The family of concurrent logic programming languages

Ehud Shapiro
September 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 3
Publisher: ACM Press
Full text available: pdf(9.62 MB) Additional Information: full citation, abstract, references, citings, index terms

Concurrent logic languages are high-level programming languages for parallel and distributed systems that offer a wide range of both known and novel concurrent programming techniques. Being logic programming languages, they preserve many advantages of the abstract logic programming model, including the logical reading of programs and computations, the convenience of representing data structures with logical terms and manipulating them using unification, and the amenability to metaprogrammin ...

8 Error detection for adaptive computing architectures in spacecraft applications

David Brodrick, Anwar Dawood, Neil Bergmann, Melanie Wark
January 2001 **Australian Computer Science Communications , Proceedings of the 6th Australasian conference on Computer systems architecture ACSAC '01**, Volume 23 Issue 4
Publisher: IEEE Computer Society , IEEE Computer Society Press
Full text available: pdf(803.02 KB) Publisher Site Additional Information: full citation, abstract, references

The Australian FedSat satellite will incorporate a payload to validate the use of adaptive computing architectures in spacecraft applications. The technology has many exciting benefits for deployment in spacecraft, but the space environment also represents unique challenges which must be addressed. An important consideration is that modern SRAM Field Programmable Gate Arrays (FPGAs), such as the Xilinx 4000 device used on FedSat,

are vulnerable to a range of radiation induced errors. A system is ...

9 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Publisher: ACM Press

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

10 IS '97: model curriculum and guidelines for undergraduate degree programs in information systems

Gordon B. Davis, John T. Gorgone, J. Daniel Couger, David L. Feinstein, Herbert E. Longenecker

December 1996 **ACM SIGMIS Database , Guidelines for undergraduate degree programs on Model curriculum and guidelines for undergraduate degree programs in information systems IS '97**, Volume 28 Issue 1

Publisher: ACM Press

Full text available: pdf(7.24 MB) Additional Information: full citation, citings

11 Data base directions: the next steps

John L. Berg

November 1976 **ACM SIGMOD Record , ACM SIGMIS Database**, Volume 8 , 8 Issue 4 , 2

Publisher: ACM Press

Full text available: pdf(9.95 MB) Additional Information: full citation, abstract

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Keywords: DBMS, auditing, cost/benefit analysis, data base, data base management, government regulation, management objectives, privacy, security, standards, technology assessment, user experience

12 Complexity and expressive power of logic programming

Evgeny Dantsin, Thomas Eiter, Georg Gottlob, Andrei Voronkov

September 2001 **ACM Computing Surveys (CSUR)**, Volume 33 Issue 3

Publisher: ACM Press

Full text available: pdf(552.99 KB) Additional Information: full citation, abstract, references, citings, index terms

This article surveys various complexity and expressiveness results on different forms of logic programming. The main focus is on decidable forms of logic programming, in particular, propositional logic programming and datalog, but we also mention general logic programming with function symbols. Next to classical results on plain logic programming (pure Horn clause programs), more recent results on various important extensions of logic programming are surveyed. These include logic programming wit ...

Keywords: Complexity, datalog, expressive power, logic programming, nonmonotonic logic, query languages

13 Middleware for mobility: Dynamically programmable and reconfigurable middleware services

Manuel Roman, Nayeem Islam

October 2004 **Proceedings of the 5th ACM/IFIP/USENIX international conference on Middleware**

Publisher: Springer-Verlag New York, Inc.

Full text available: pdf(651.39 KB) Additional Information: full citation, abstract, references

The increasing software complexity and proliferation of distributed applications for cell phones demand the introduction of middleware services to assist in the development of advanced applications. However, from the user perspective, it is essential that these new phones provide a smooth error-free experience. Despite of the complexity underlying a cell phone, placing a phone call remains a simple task that can be performed by most users regardless of their technical background. Furthermore, ce ...

14 Special issue on on inductive logic programming: Learning semantic lexicons from a part-of-speech and semantically tagged corpus using inductive logic programming

Vincent Claveau, Pascale Sébillot, Cécile Fabre, Pierrette Bouillon

December 2003 **The Journal of Machine Learning Research**, Volume 4

Publisher: MIT Press

Full text available: pdf(215.86 KB) Additional Information: full citation, abstract, references, index terms

This paper describes an inductive logic programming learning method designed to acquire from a corpus specific Noun-Verb (N-V) pairs---relevant in information retrieval applications to perform index expansion---in order to build up semantic lexicons based on Pustejovsky's generative lexicon (GL) principles (Pustejovsky, 1995). In one of the components of this lexical model, called the qualia structure, words are described in terms of semantic roles. For example, the <em&g ...

15 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science

William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young

March 1968 **Communications of the ACM**, Volume 11 Issue 3

Publisher: ACM Press

Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

16 Draft Proposed: American National Standard—Graphical Kernel System

Technical Committee X3H3 - Computer Graphics

February 1984 **ACM SIGGRAPH Computer Graphics**, Volume 18 Issue SI

Publisher: ACM Press

Full text available: pdf(16.07 MB) Additional Information: full citation

17 Special session on reconfigurable computing: Designing and testing fault-tolerant

techniques for SRAM-based FPGAs
Fernanda Lima Kastensmidt, Gustavo Neuberger, Luigi Carro, Ricardo Reis
April 2004 **Proceedings of the 1st conference on Computing frontiers**
Publisher: ACM Press
Full text available: pdf(390.51 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses fault-tolerant techniques for SRAM-based FPGAs. These techniques can be based on circuit level modifications, with obvious modifications in the programmable architecture, or they can be implemented at the high-level description, without modification in the FPGA architecture. The high-level method presented in this work is based on Triple Modular Redundancy (TMR) and a combination of Duplication Modular Redundancy (DMR) with Concurrent Error Detection (CED) techniques, which ...

Keywords: FPGA, fault-tolerance

18 Guidance for the use of the Ada programming language in high integrity systems
B. A. Wichmann
July 1998 **ACM SIGAda Ada Letters**, Volume XVIII Issue 4
Publisher: ACM Press
Full text available: pdf(2.93 MB) Additional Information: full citation, abstract, citings, index terms

This paper is the current result of a study by the ISO HRG Rapporteur group which is being circulated for comment. Many people have contributed to this, but those who have either attended two recent meetings of group or have made substantial e-mail comments are: Praful V Bhansali (Boeing, USA), Alan Burns (University of York, UK), Bernard Carre' (Praxis Critical Systems, UK), Dan Craigen (ORA, Canada), Nick Johnson MoD, UK), Stephen Michell (Canada), Gilles Motet (DGEI/INSA, France), George Roma ...

19 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Publisher: ACM Press
Full text available: pdf(5.28 MB) Additional Information: full citation

20 Conference abstracts
January 1977 **Proceedings of the 5th annual ACM computer science conference**
Publisher: ACM Press
Full text available: pdf(3.14 MB) Additional Information: full citation, abstract, index terms

One problem in computer program testing arises when errors are found and corrected after a portion of the tests have run properly. How can it be shown that a fix to one area of the code does not adversely affect the execution of another area? What is needed is a quantitative method for assuring that new program modifications do not introduce new errors into the code. This model considers the retest philosophy that every program instruction that could possibly be reached and tested from the ...

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
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Yamada, Y.; Watanabe, T.; Muroga, T.; Miyata, S.; Iwai, H.; Ibi, A.; Shiohara, Y Hirayama, T.;
Applied Superconductivity, IEEE Transactions on
Volume 15, Issue 2, Part 3, June 2005 Page(s):2600 - 2603
Digital Object Identifier 10.1109/TASC.2005.847666
AbstractPlus | References | Full Text: PDF(992 KB) **IEEE JNL**

2. **Configurable fault-tolerant processor (CFTP) for spacecraft onboard proc**
Hulme, C.A.; Loomis, H.H.; Ross, A.A.; Rong Yuan;
Aerospace Conference, 2004. Proceedings. 2004 IEEE
Volume 4, 6-13 Mar 2004 Page(s):2269 - 2276 Vol.4
Digital Object Identifier 10.1109/AERO.2004.1368020
AbstractPlus | Full Text: PDF(608 KB) **IEEE CNF**

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6-8 Nov. 2002 Page(s):60 - 68
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4. **Synthesis challenges for next-generation high-performance and high-der**
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25-28 Jan. 2000 Page(s):157 - 162
Digital Object Identifier 10.1109/ASPDAC.2000.835088
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5. **Run-time reconfiguration: towards reducing the density requirements of**
Brunham, K.; Kinsner, W.;
Electrical and Computer Engineering, 2001. Canadian Conference on
Volume 2, 13-16 May 2001 Page(s):1259 - 1264 vol.2
Digital Object Identifier 10.1109/CCECE.2001.933623
AbstractPlus | Full Text: PDF(420 KB) **IEEE CNF**

☐ **6. An overview of technology, architecture and CAD tools for programmabl**
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Custom Integrated Circuits Conference, 1994., Proceedings of the IEEE 1994
1-4 May 1994 Page(s):69 - 76
Digital Object Identifier 10.1109/CICC.1994.379764
AbstractPlus | Full Text: PDF(788 KB) **IEEE CNF**

☐ **7. Enhanced reliability of finite-state machines in FPGA through efficient fa correction**
Tiwari, A.; Tomko, K.A.;
Reliability, IEEE Transactions on
Volume 54, Issue 3, Sept. 2005 Page(s):459 - 467
Digital Object Identifier 10.1109/TR.2005.853438
AbstractPlus | Full Text: PDF(408 KB) **IEEE JNL**

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Wei-Je Huang; Mitra, S.; McCluskey, E.J.;
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Symposium on
24-26 Oct. 2001 Page(s):206 - 214
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Seals, R.C.;
Programmable Logic Devices for Digital Systems Implementation, IEE Colloqu
25 May 1990 Page(s):3/1 - 3/3
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☐ **10. High rate deposition by PLD of YBCO films for coated conductors**
Watanabe, T.; Kuriki, R.; Iwai, H.; Muroga, T.; Miyata, S.; Ibi, A.; Yamada, Y.;
Applied Superconductivity, IEEE Transactions on
Volume 15, Issue 2, Part 3, June 2005 Page(s):2566 - 2569
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AbstractPlus | References | Full Text: PDF(984 KB) **IEEE JNL**

☐ **11. Continuous deposition and rapid fabrication of self-epitaxial CeO/sub 2/ PLD method on IBAD buffers**
Muroga, T.; Miyata, S.; Watanabe, T.; Ibi, A.; Yamada, Y.; Shiohara, Y.;
Applied Superconductivity, IEEE Transactions on
Volume 15, Issue 2, Part 3, June 2005 Page(s):2695 - 2698
Digital Object Identifier 10.1109/TASC.2005.847785
AbstractPlus | References | Full Text: PDF(184 KB) **IEEE JNL**

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Dobias, R.; Kubatova, H.;
Digital System Design, 2004. DSD 2004. Euromicro Symposium on
31 Aug.-3 Sept. 2004 Page(s):467 - 473
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